Iranian Journal of Science & Technology, Transaction B: Engineering, Vol. 33, No. B6, pp 477-490
Printed in The Islamic Republic of Iran, 2009

COMPREHENSIVE CONTROL SCHEME FOR AN INVERTER-BASED DISTRIBUTED GENERATION UNIT*

E. ROKROK AND M. E. HAMEDANI GOLSHAN**

Dept. of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, I. R. of Iran
Email: hgolshan@cc.iut.ac.ir

Abstract– In this paper, a complete control scheme is developed for an inverter-based distributed generation (IBDG) unit to produce high quality AC voltages in unit terminals. The unit uses a three-phase, four-leg inverter. The control scheme includes a feed-forward current control path and two nested loops, the outer loop for regulating the DG output voltage and the inner one for controlling the inverter current. Proportional-Resonant (PR) controllers are used in the voltage loop to track a sinusoidal reference voltage and eliminate low-order voltage harmonics. The inner current loop is used for over-load protection of the inverter, and improvement of the control system response. The current controller is designed by the state feedback method. The feed forward current control path is used to reduce impacts of load disturbances on the IBDG output voltages. Regarding the role of the inverter output filter and controllers in voltage quality, the filter design procedure is reviewed, the approach to choosing the controllers parameters is explained, and stability conditions of the system are investigated. The performance of an IBDG that supplies a local load is studied under unbalanced and nonlinear loading, and sudden changes in the load amount and voltage amplitude.

Keywords– Distributed generation, unbalanced loading, nonlinear load, four-leg inverter, proportional-resonant controller, feed-forward current control path

1. INTRODUCTION

In recent years, distributed generations have been increasingly employed to supply local loads or low/medium voltage grids. Many of these resources require a power electronic interface to export power to 50 or 60 Hz grids or local loads. Generally, for obtaining high quality sinusoidal voltage waveforms in the IBDG output, the following are required:

- An IBDG should generate three independent phase voltages when it is used to supply unbalanced and nonlinear loads. Then, an appropriate inverter configuration such as a three-phase, four-leg inverter should be employed. This inverter can produce high quality sinusoidal voltage waveforms by providing zero sequence voltage and multiples of the third harmonic voltage.
- The pulse-width modulated (PWM) inverter requires high switching frequency to provide sufficient control band-width. Then, disturbances due to the presence of extreme levels of unbalanced and harmonically distorted load currents can be rejected by using a well-designed control system.
- The inverter requires an output low-pass filter such as an LC filter to reduce the inverter output current ripple and attenuate high frequency voltage components due to switching.
- A proper control scheme is required to track the reference command, to balance the output voltages and to eliminate the low-order harmonic components.

*Received by the editors July 20, 2008; Accepted August 27, 2009.
**Corresponding author

Many IBDG control strategies, such as the PI controller in dq0 synchronous frame [1], optimal state feedback control [2], optimal servo mechanism control [3], and robust control [4], have been proposed to produce sinusoidal voltages according to the related standards such as IEEE-1547 [5]. PI controller has a simple structure and provides good performance in reference command tracking when signals are stationary or pseudo-stationary [6]. Thus, it can be used as the voltage/current controller of IBDG in the dq0 synchronous frame. However, because of the presence of harmonics in the system variables due to the inverter switching process and nonlinear loads, the reference command cannot be tracked precisely. Although reference command tracking can be improved by increasing the proportional gain of the PI controller, it leads to a reduced system stability margin. In addition, in order to attenuate the effects of unbalanced and harmonically distorted load currents on the source output voltages, using multiple synchronous frames is necessary. Optimal state feedback control has been utilized for a three-leg inverter that supplies a balanced and linear load [2]. The state feedback controller is designed based on the exact model of the system. The model can be very complicated and may not always be available. The control actions produced by this controller are often big. When they are limited by the reference voltage/current limiter blocks, optimal performance of the control system is violated. In [3], optimal servo mechanism control has been utilized to eliminate specified unwanted voltage harmonics from the three-leg inverter output voltages. The servo mechanism controller usually has a high order and large band-width. In addition, sensitivity of the controller to the system parameter variations is usually high. In [4], H_∞ controller has been designed for voltage regulating of a DC/AC converter under balanced and linear loading conditions. The controller is robust against variations of filter capacitance caused by power factor compensation of the system loads. In [7], a PR controller was employed for a grid-connected voltage-source converter. The PR controller was extended to parallel inverter and its superior performance over the Proportional-Integral-Derivative (PID) controller was shown in [8]. It was shown that one PR controller in a stationary frame is equivalent to two PI controllers related to positive and negative sequence components in synchronous frames. Proportional-Resonant (PR) controller has high computational efficiency because it is performed in a stationary frame and there is no need for frame transformations. It has a good performance in reference signal tracking when the reference signal is a sinusoidal waveform. Less dependence on the system model and good robustness against system parameters variations are other advantages of the PR controller.

In this paper, PR controllers are used to track sinusoidal voltage reference and eliminate the low-order voltage harmonics in a four-leg inverter-based DG supplying a local load. For limiting the inverter current under overload or fault conditions and improving the performance of the voltage control loop, an inner current control loop is used too. Current controller is designed by state feedback method because of the good performance in reference command tracking and its fast response and computational efficiency [9]. In addition, to enhance the ability of the control system in the rejection of load disturbances, a feed-forward current control path is used for the IBDG. It effectively decreases the source output impedance at the fundamental and low frequencies. The proposed control scheme presents a good performance in voltage reference tracking, low-order voltage harmonics elimination and load disturbance rejection under nonlinear and unbalanced loading conditions. In addition, it has good robustness against system parameters variations. Proper design of the inverter filter significantly affects the improvement of the IBDG voltage quality. The filter must effectively attenuate the high frequency voltage harmonics that are out of the voltage control loop band-width. Design procedures for the controllers and the inverter output filter are explained and the necessary conditions for stability of the control system are investigated. The performance of the proposed IBDG consisting of a four-leg inverter with its output filter and control configuration is studied under unbalanced and nonlinear loading and sudden changes in the load amount and reference voltage amplitude.

2. INVERTER CONFIGURATION

Figure 1 shows the configuration of a four-leg inverter and its output LC filter. The switching strategy is sinusoidal pulse-width modulation (SPWM) selected according to [10]. In this method, the reference voltage vector produced by the controller is projected onto the axes of a non-orthogonal stationary a-b-c-n frame in order to generate phases and neutral voltage references for the inverter. According to these voltage references, SPWM modulator generates gate signals to excite the inverter legs. It is possible to provide three independent phase voltages in the output terminals of the four-leg inverter.

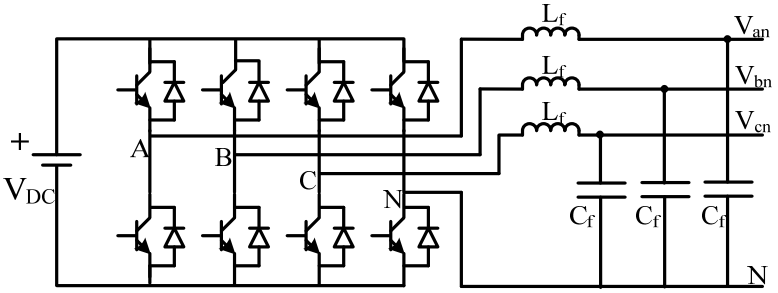

Fig. 1. Four-leg inverter with output filter

Actually, this configuration acts similar to three independent single-phase inverters. Because of the presence of a neutral line in this configuration, the output-filtered voltages can be directly connected to a single-phase or a three- phase load without any need for an insulating transformer.

3. CONTROL SYSTEM STRUCTURE

Figure 2 shows the control system structure. As can be seen, the control system calculations are performed in the stationary α-β-0 frame. Voltages and currents are measured in the stationary a-b-c-n frame, and transferred to the orthogonal α-β-0 frame. For each α, β and 0 direction, there is an independent controller that provides control signals in the same direction. Inverter reference voltage vector is constructed by the outputs of these controllers, and transferred back to the a-b-c-n frame to provide phase and neutral voltage references for the four-leg inverter. In each control direction there are two nested loops, an outer loop for voltage reference tracking and low-order voltage harmonics elimination, and an inner current control loop for protection of the inverter against overload and for improvement of the control system response. In addition, for reducing the load disturbance effects on IBDG output voltages, a feed-forward current control path is used.

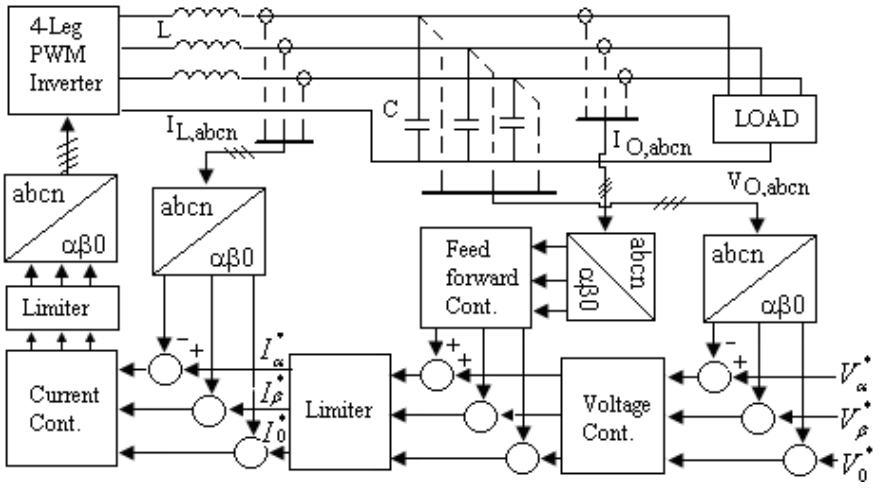

Fig. 2. Control system structure

In modeling and analyzing a voltage source inverter, the inverter and its PWM modulator are usually modeled as a constant gain at frequencies much smaller than switching frequency.

a) Current controller

Current controller is employed for regulating the inverter current, protecting the inverter against overload, and improving the overall control system response. The inverter current reference is constructed by voltage controller and feed-forward current control path. For limiting the inverter output current to a certain level, a limiter block is used in the reference current path (Fig. 2). This current level is determined by nominal current of the inverter switches. It is usually chosen as two times the inverter nominal current [11]. The performance of control system is improved when a current control loop is used along with the voltage control loop since more state variables participate in the control system in comparison to the case that there is only voltage control loop. However, an improper design of the current control loop can decrease the stability margin of the control system, or even force it toward instability. In this work, the current controller is designed by state feedback method [9]. Deriving current controller equation is started from the inductor current equation of the LC filter

$$\frac{di_{Lf}}{dt} = -\frac{r_f}{L_f} i_{Lf} - \frac{1}{L_f} v_c + \frac{1}{L_f} v_{in} \tag{1}$$

where L_f, r_f, i_{Lf}, v_c and v_{in} are inductance of LC filter, resistance of inductor, inductor current, capacitor voltage and inverter output voltage, respectively. By ignoring the switching model of the inverter at low frequency range, and assuming unity gain for the inverter and its PWM modulator, v_{in} is considered as an output of the current controller. By defining the error of reference current tracking as

$$e_I = i_{L,ref} - i_{Lf} \tag{2}$$

and substituting (2) in (1), we obtain

$$\frac{di_{L,ref}}{dt} - \frac{de_I}{dt} = -\frac{r_f}{L_f} i_{Lf} - \frac{1}{L_f} v_c + \frac{1}{L_f} v_{in} \tag{3}$$

If the current controller equation is considered as

$$v_{in} = v_c + L_f \frac{di_{L,ref}}{dt} + ke_I \tag{4}$$

the error of reference current tracking will tend to zero. In Eq. (4), k is a constant gain selected to adjust the band-width of the current control loop. The inverter switching frequency determines the band-width of the current control loop. For attaining a proper transfer function for the inner current control loop, an approximate relation for the derivative of the current reference command is used in the current controller equation. Thus, Eq. (4) in the frequency domain is written as

$$v_{in} = v_c + L_f \frac{s}{1+\tau s} i_{L,ref} + ke_I \tag{5}$$

where $1/\tau$ is selected several times greater than the fundamental frequency [11].

b) Voltage controller

PR controller is used for controlling the IBDG voltage. Transfer function of a PR controller is given by

$$H_{PR}(s) = k_p + \frac{k_i s}{s^2 + \omega_0^2} \tag{6}$$

where ω_0, k_p and k_i are resonant frequency, proportional and integral gains of controller, respectively. According to internal model principle, if the resonant frequency of the PR controller is equal to the frequency of a sinusoidal reference voltage, then the controller introducing an infinite gain at this frequency makes the DG output voltage track the reference command. By employing a number of other PR controllers parallel to the reference voltage tracking PR controller, the low frequency voltage harmonics whose frequencies are in the range below the voltage control loop band-width can be eliminated. The resonant frequencies of these controllers are selected equal to one of the components that should be eliminated. Coefficients k_p and k_i in a PR controller are similar to those in a PI controller, and should be adjusted to set an appropriate frequency response to the voltage control loop [12]. For achieving the control objectives and modeling the inverter and its PWM modulator as a constant gain, the control voltage loop band-width is chosen much lower than the switching frequency of the inverter.

Equation (6) gives an ideal PR controller because of its infinite gain at angular frequency ω_0. Since the gain of ideal PR controller at the resonant frequency is highly sensitive to frequency deviation, a large error may be introduced in the tracking reference signal for any small deviation of reference signal frequency. To overcome this problem, a non-ideal PR controller with transfer function (7) can be used

$$H_{aPR}(s) = k_p + \frac{k_i \omega_{cut} s}{s^2 + 2\omega_{cut} s + \omega_0^2} \tag{7}$$

where ω_{cut} is the controller cut-off frequency. Although using non-ideal PR controller increases the error of reference tracking in the resonant frequency, it can reduce the sensitivity of the controller to frequency deviations. Choosing ω_{cut} is the compromise between reduction of the sensitivity and tracking error**.** For avoiding interaction between the voltage and current control loops, and ensuring system stability, the band-width of the voltage control loop must be selected several times lower than the current loop band-width.

c) Feed-forward current control path

Feed-forward current control path is used for decreasing impacts of load disturbances on DG output voltages through reducing its output impedance. A block diagram of a control system in one direction is shown in Fig. 3. In this figure, the PR controllers used for eliminating low-order voltage harmonics are not shown. Function F(s) in the feed- forward path is a low-pass filter whose input is load current, and whose output is used as a partition of the inverter current reference. F(s) has a gain equal to or a little less than unity, and approximately a zero phase angle at low frequency ranges from zero to the fundamental system frequency. Employing feed-forward control path results in a reduced output impedance of the source at low frequencies. Decreasing source output impedance increases its voltage robustness against load disturbances.

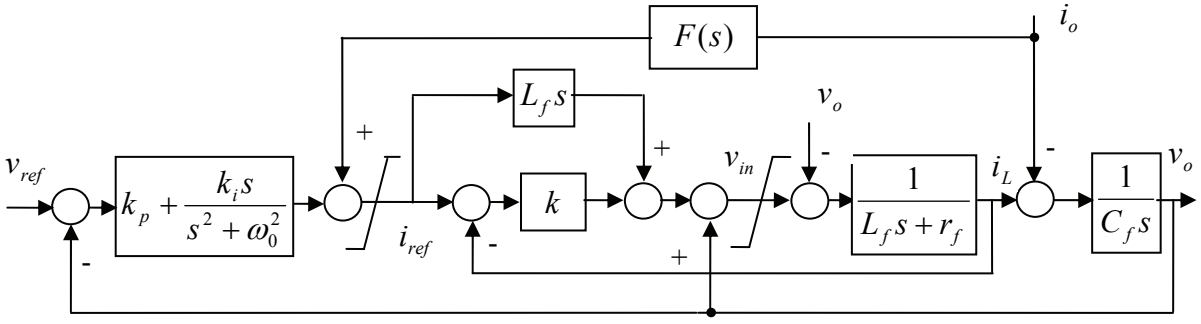

Fig. 3. Block diagram of control system in one direction

4. VOLTAGE TRANSFER FUNCTION AND OUTPUT IMPEDANCE OF IBDG

By using a block diagram of the control system indicated in Fig. 3, voltage transfer function and output impedance of IBDG can be obtained. To simplify the analysis, only the PR controller associated with the voltage reference tracking is considered and F(s) is substituted by constant unity gain. These simplifications do not change the overall system behavior. In simulation of the system, function F(s) and PR controllers associated with the voltage harmonics elimination are precisely considered. Based on the simplified block diagram in Fig. 3, the relationship between DG output voltage, voltage reference and load current is given by

$$V_o(s) = G(s).V_{ref}(s) - Z(s).I_o(s) \tag{8}$$

where G(s) and Z(s) are voltage transfer function and output impedance, respectively, to be expressed by (9) and (10). The characteristic equation of control system is expressed by (11). Stability of the control system can be determined by applying Roth stability criteria to the characteristic equation. Frequency design methods based on Bode plots are used to obtain the parameters of the voltage controller [11].

$$G(s) = \frac{(L_f s + k)(k_p s^2 + k_i s + k_p \omega_0^2)}{L_f C_f s^4 + [C_f(k + r_f) + k_p L_f]s^3 + (L_f C_f \omega_0^2 + k_p k + k_i L_f)s^2 + [(kC_f + r_f C_f + k_p L_f)\omega_0^2 + kk_i]s + kk_p \omega_0^2} \tag{9}$$

$$Z(s) = \frac{(s^2 + \omega_0^2).[r_f + k(1 - F(s)) + L_f s(1 - F(s))]}{L_f C_f s^4 + [C_f(k + r_f) + k_p L_f]s^3 + (L_f C_f \omega_0^2 + k_p k + k_i L_f)s^2 + [(kC_f + r_f C_f + k_p L_f)\omega_0^2 + kk_i]s + kk_p \omega_0^2} \tag{10}$$

$$L_f C_f s^4 + [C_f(k + r_f) + k_p L_f]s^3 + (L_f C_f \omega_0^2 + k_p k + k_i L_f)s^2 + [(kC_f + r_f C_f + k_p L_f)\omega_0^2 + kk_i]s + kk_p \omega_0^2 = 0 \tag{11}$$

As Eq. (9) tells us, if the voltage transfer function is stable and its bandwidth is much lower than the switching frequency of the inverter, the inverter output voltage will exactly track a sinusoidal reference input voltage with frequency ω_0. In addition, Eq. (9) shows that feed-forward current control path has no impact on the voltage transfer function. It can be seen from (10) that feed-forward current control path decreases the output impedance of the source significantly. At the fundamental frequency, the source output impedance is zero.

5. CHOOSING FILTER AND CONTROLLER PARAMETERS

Inverter switching frequency is chosen based on a trade-off between acceptable switching losses and control band-width and also, the cost and size of the filter components. Regardless of the inverter control system**,** the LC filter parameters are chosen such that the unwanted components in the inverter output voltage are attenuated effectively and inverter current ripple is reduced admissibly by some methods such as the one presented in [13]. The inductance value of the filter is chosen to obtain a specified level of ripple for the inverter current. Larger values of the inductance lead to lower inverter current ripple at the cost of a higher DC link voltage and the larger current control loop gain. The capacitance value is determined to achieve a low impedance value for the capacitor at the switching frequency and a high impedance value at fundamental frequency of the system. In fact, the filter must have a high attenuation factor at the switching frequency to attenuate the high frequency switching components effectively.

A common rule of thumb for choosing the filter parameters is to achieve attenuation factor 100 at the switching frequency [14].

$$\left|\frac{Z_c(j\omega_s)}{Z_c(j\omega_s)+Z_L(j\omega_s)}\right| = \frac{1}{100} \tag{12}$$

where Z_c, Z_L are the capacitor and inductor impedances, respectively and ω_s denotes inverter switching frequency. This requires that filter resonant frequency, ω_{L-C}, be about 0.1 of the inverter switching frequency, ω_s. Therefore, after specifying filter inductance, capacitance value is determined by Eq. (13)

$$\omega_{L-C} = \frac{1}{\sqrt{L.C}} \tag{13}$$

In IBDG modeling, the switching process of the inverter is usually ignored and PWM modulator is considered as a constant gain. To validate this assumption, the inner current control loop bandwidth must be several times lower than the inverter switching frequency. Transfer function of the inner current control loop is obtained from Fig. 3 as

$$G_i(s) = \frac{(k.\tau + L_f)s + k}{\tau.L_f.s^2 + [L_f + \tau.(k + r_f)].s + (k + r_f)} \tag{14}$$

The current controller gain, *k*, determines the bandwidth of the inner current control loop. It is selected based on the switching frequency of the inverter. If a band-width of $G_i(s)$ is considered as one third of the inverter switching frequency, then *k* of approximately 20(V/A) will be obtained.

In the next step, the voltage control loop should be designed with a bandwidth that is at least three times slower than that of the inner current loop to preserve the stability and tracking resolution of the reference current command [15]. The parameters of the voltage controller, k_p ,k_i, are determined to attain desirable frequency responses of the voltage closed-loop transfer function, *G(s)*. Desirable specifications of the frequency responses are as follows:

1. Stability of the voltage closed-loop transfer function.
2. Enough phase and gain margins.
3. Unit magnitude and zero phase at fundamental frequency and harmonic frequencies that must be eliminated.
4. Frequency bandwidth of *G(s)* must be at least one decade less than the inverter switching frequency.

A parameter adjustment approach such as frequency design methods can be used for determining voltage controller parameters [12].

Feed-forward current control path is employed to enhance the ability of the control system to reject load disturbances. Based on the impedance transfer function, Z(s), the feed-forward controller, *F(s)*, is chosen as a first order low-pass filter with unity gain and cut-off frequency that should be several times greater than the fundamental frequency of the system. One option can be:

$$F(s) = \frac{w_c}{s + w_c}\ ,\ w_c = 7 \times (2\pi f_0) \tag{15}$$

By considering the above-explained criteria and a little bit of trial and error, the filter and controller parameters have been determined for an IBDG that supplies a local load. Table 1 shows the chosen parameters and specifications of DG. The system frequency responses are observed in Figs. 4 and 5, showing Bode plots of the voltage transfer function and the source output impedance.

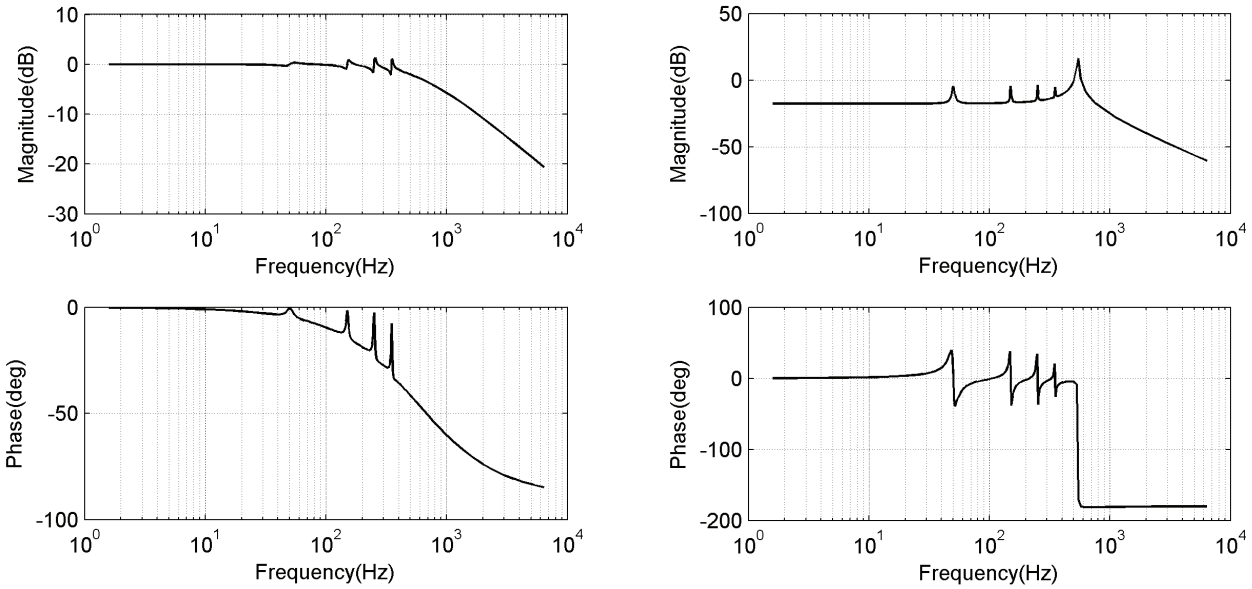

Fig. 4. Bode plots of the voltage transfer function in the case of (a) using the current control loop, and (b) not using the current control loop

In this study, non-ideal PR controllers for the fundamental component and the third, fifth and seventh harmonics have been employed. The effect of the current control loop on the voltage reference tracking and voltage harmonics attenuation is observed by comparing Bode plots of the voltage transfer function in the case of using and not using the current control loop shown in Figs. 4.a and 4.b, respectively. Fig. 4.a demonstrates appropriate voltage reference tracking and voltage harmonics attenuation.

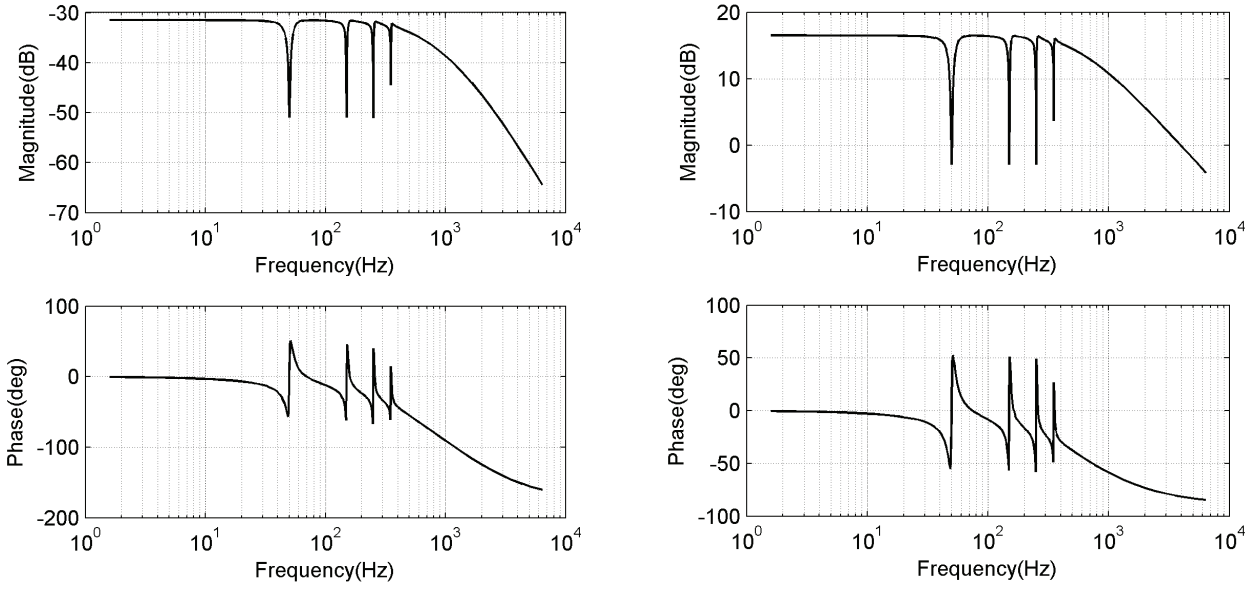

Fig. 5. Bode plots of the source output impedance (a) with the feed-forward current control path, and (b) without the feed-forward current control path

In addition, Figs. 5a and 5b show Bode plots of the source output impedance with and without the feed-forward current control path, respectively, indicating the effect of the feed-forward control path. High ability of the control system for the rejection of load disturbances results from low output impedance of the source as shown in Fig. 5a.

6. PROPOSED CONTROL SYSTEM PERFORMANCE

The performance of the proposed control system has been investigated for the parameters specified in Table 1 under different loading conditions by using simulations performed in Matlab/Simulink environment.

Table 1. The control system parameters

Power rating	50kVA
System frequency	50Hz
Switching frequency	5kHz
L_f	2.5mH
C_f	40μF
r_f	0.2Ω
k	20(V/A)
k_p	0.5(A/V)
k_i	10(A/V.S)
ω_{cut}	10(rad/s)
$V_{L\text{-}L}$	380V
Vdc	800V

For observing the impact of inner current loop on the improvement of load voltage quality and dynamic response of the control system, the system behavior is studied in the absence and presence of the inner current control loop.

a) IBDG performance in the absence and presence of inner current control loop

In this study and in the absence of the inner current control loop, the linear and balanced three-phase load connected to DG is changed from 20 kW to 50 kW at t= 0.05 sec, then returned back to the initial value at t=0.1 sec. Figs. 6a, 6b and 6c show the produced voltage at one phase of inverter output, load voltages and load currents, respectively. As observed in these figures, the quality of load voltages is not acceptable and there are considerable oscillations in load voltages under light loading conditions.

These load conditions are considered for DG in the presence of the inner current control loop and feed-forward control path. Figs. 7a, 7b and 7c show the produced voltage in one phase of the inverter, load voltages and load currents, respectively. It is observed that there is a high quality voltage under all loading amounts. In addition, the control system presents an excellent dynamic response to sudden load variations.

b) IBDG performance in the case of unbalanced load

In this study, a 40kW three-phase load and a 10kW single-phase load are connected to the IBDG outputs. Figs. 8a and 8b show currents and voltages of the unbalanced load. As observed in these figures, although a severely unbalanced load has been connected to the source, the load voltages present a balanced set. This result is due to the proper configuration of the inverter and well-designed controllers and filter. The frequency spectrum, calculated for one cycle of the load phase voltages by discrete Furrier transform, is shown in Fig. 8c.

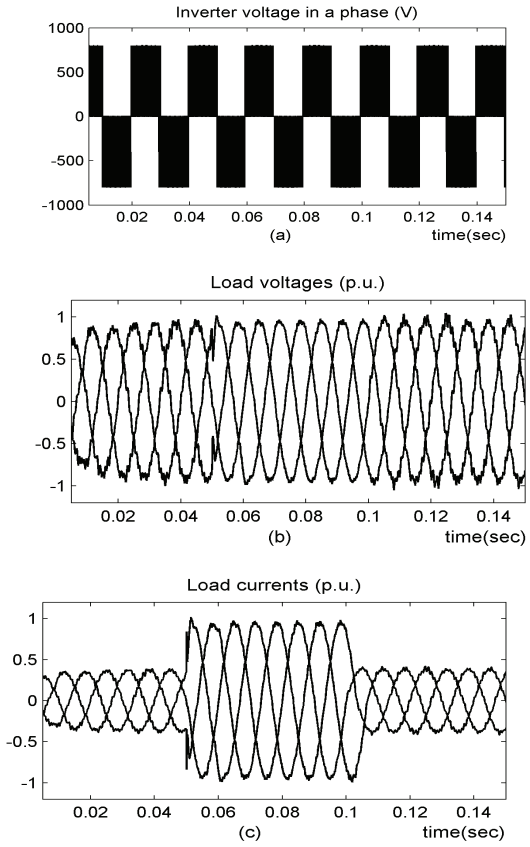

Fig. 6. IBDG performance in absence of the inverter current control loop (a) produced voltage in one phase of the inverter (b) load voltages (c) load currents

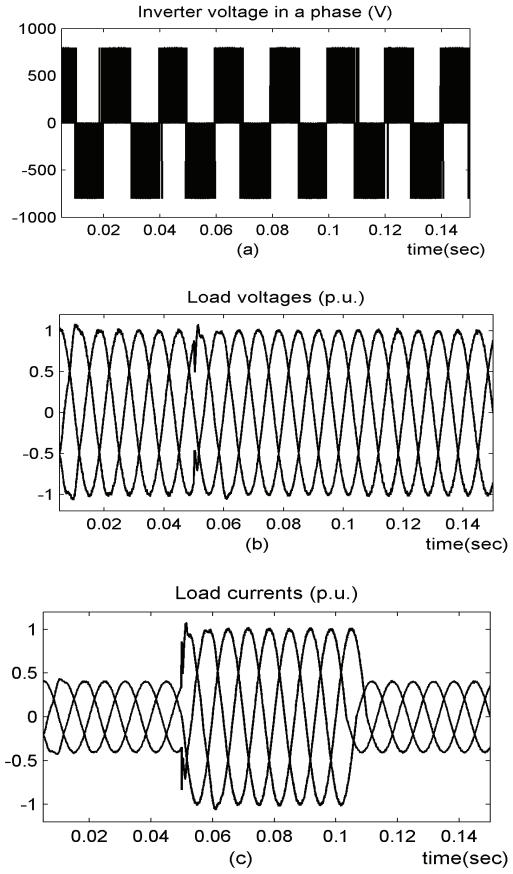

Fig. 7. IBDG performance in the presence of the inverter current control loop (a) produced voltage in one phase of the inverter (b) load voltages (c) load currents

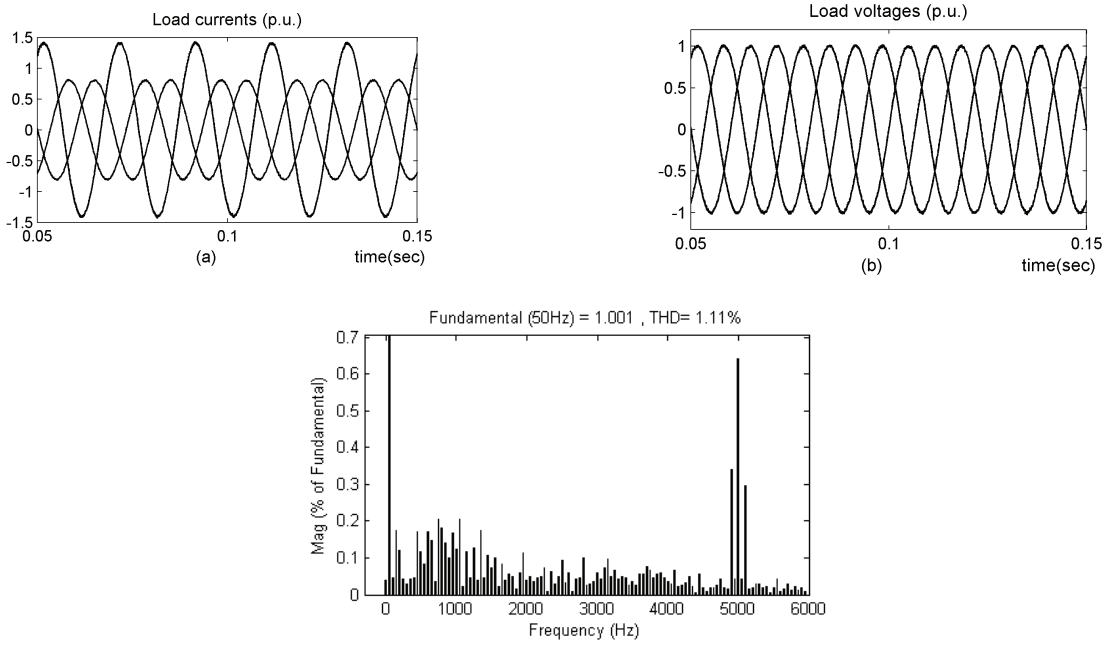

Fig. 8. Unbalanced loading (a) load currents (b) load voltages (c) load voltage frequency spectrum

As observed, the total harmonic distortion (THD) value of the load voltages is very small in this loading condition.

c) IBDG performance in the case of nonlinear load

In this case, a nonlinear load, consisting of three fully controlled single-phase rectifiers that supply 1.5 ohm resistors, has been connected to the source. The load currents include high levels of the 3rd, 5th, and 7th harmonics. In Figs. 9a, 9b current and voltages of the nonlinear load are depicted. As observed in Fig. 9b, although the source supplies a severely nonlinear load, the load voltages are almost like sinusoidal waveforms. This result is due to proper configuration of the inverter and appropriate control structure and filter. Figs. 9c and 9d show frequency spectrums of one cycle of the load phase currents and voltages.

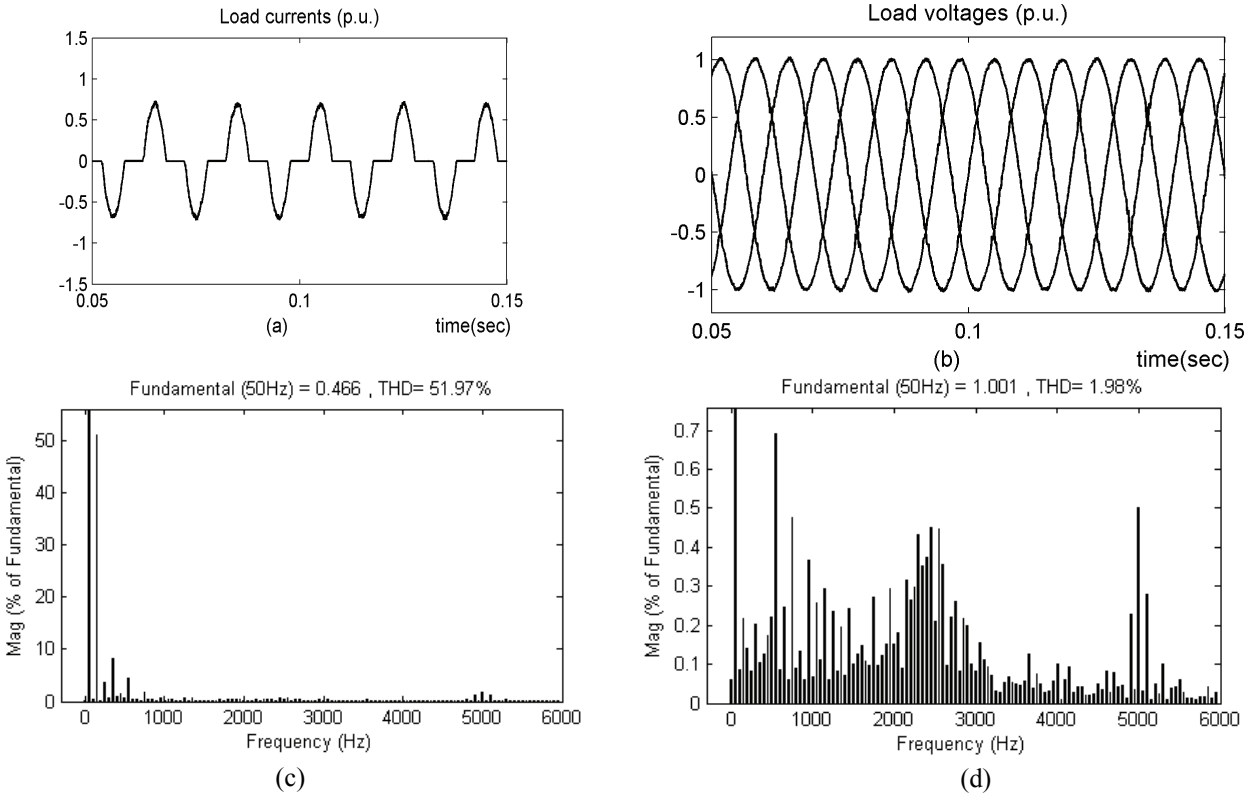

Fig. 9. Nonlinear load condition (a) load current (b) load voltages(c) frequency spectrum of load current (d) frequency spectrum of load voltage

As shown in these figures, IBDG presents very good performance under nonlinear load conditions, in view of supplying the load by high quality voltages.

d) IBDG performance in the case of filter parameters variations

In this case, while IBDG supplies a 50kW linear and balanced three-phase load, capacitance of the inverter filter is increased to twice that of the base value. As observed in Fig. 10 which shows load voltages and currents, the control system has good robustness against variations of the filter capacitance. Also, the control system has good robustness against variations of filter inductance as observed in Fig.11. This figure shows load voltages and currents for the case that the inductance of the filter is increased to twice the base value.

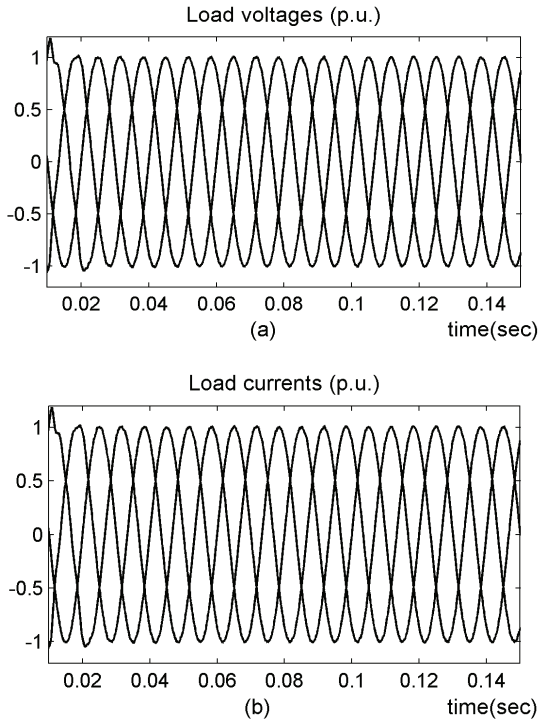

Fig. 10. (a) load voltages and (b) load currents in the case of increasing the filter capacitance to twice of the base value

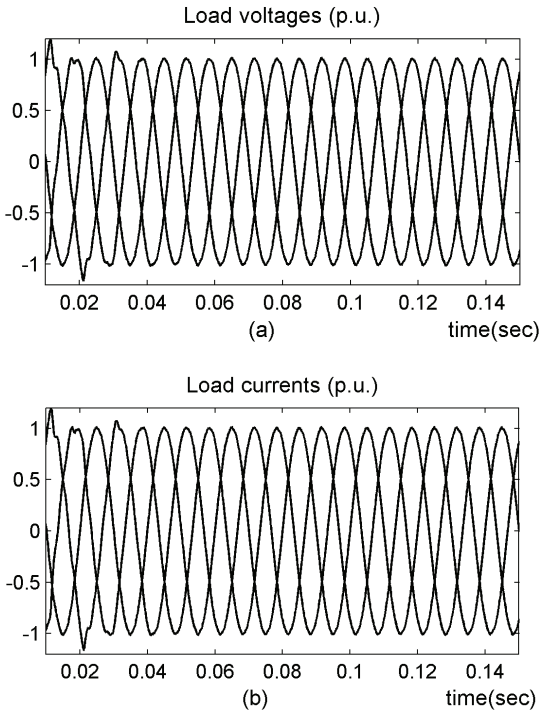

Fig. 11. (a) load voltages and (b) load currents in the case of increasing the filter inductance to twice of the base value

This result is due to an appropriate control structure and well-designed filter. Hence, the control system is robust with respect to the parameters variations of the system.

e) System control response to step changes in the voltage reference

Assume IBDG is supplying a 50kW linear and balanced three-phase load. Fig. 12 shows load voltages and currents when the amplitude of source reference voltage is changed from 1 (pu) to 0.7 (pu) at t= 0.05 sec, then returned back to the initial value at t=0.1 sec. It is observed that the control system has a good steady state and dynamic response.

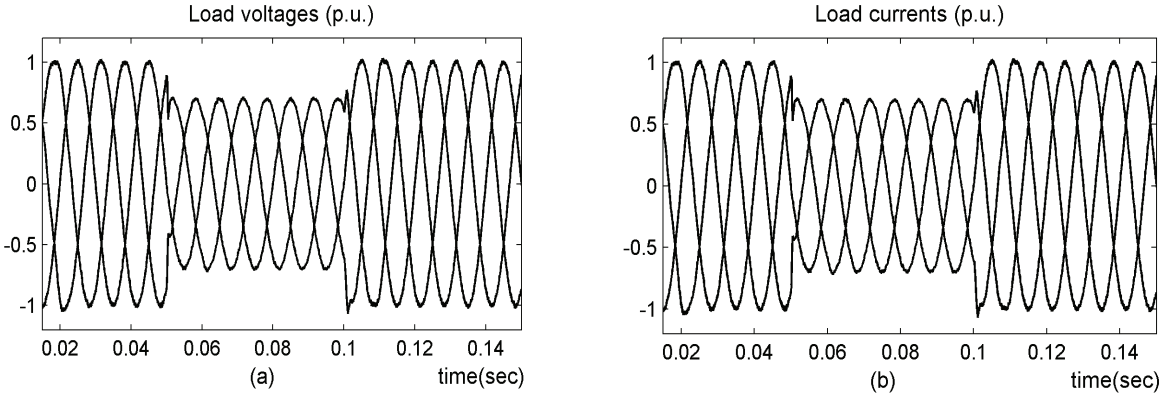

Fig. 12. The system response to a step change of voltage reference (a) load voltages (b) load currents

7. CONCLUSION

A complete control scheme including a feed-forward current control path, voltage and current control loops and appropriate controllers, PR controllers for voltage control loop and state feedback-based controller for current control loop was proposed for IBDG units. The bases and methods of the inverter filter and the controllers design have been explained. Employing four-leg inverter configuration, along with the output filter and proposed control scheme leads to the following results:

- Three independent phases to neutral voltages can be generated so that the required zero sequence and multiples of third harmonic components are provided in the inverter output voltages.
- The reference voltage is precisely tracked and voltage harmonics are effectively attenuated.
- Over-load protection is provided for the inverter.
- The control system presents excellent steady state and dynamic responses.
- The impacts of load disturbances on IBDG voltages are considerably reduced.

Generally, the source presents a high quality voltage in its output under all loading conditions and is subject to sudden variations in reference voltage and load amount. The performance of the proposed IBDG supplying a local load has been demonstrated by simulation of different loading and disturbance conditions.

REFERENCES

1. Han, B., Bae, B., Kim, H. & Baek, S. (2006). Combined operation of unified power-quality conditioner with distributed generation. *IEEE Trans. Power Deli*., Vol. 21, No.1, p. 330.
2. Botteron, F., Pinherio, H., Grundling, H. A., Pinheiro, J. R. & Hey, H. L. (2001). Digital voltage and current controllers for three-phase PWM inverter for UPS applications. *Proc. IEEE-IAS Annu. Meeting*, p. 2667.
3. Marwali, M. N & Keyhani, A. (2004). Control of distributed generation systems-Part I: Voltages and currents control. *IEEE Trans. Power Electron*. Vol. 19, No. 6, p. 1541.
4. Li, Y., Vilathgamuwa, D. M. & Loh, P. C. (2007). Robust control scheme for a microgrid with PFC capacitor connected. *IEEE Trans. Industry App*., Vol. 43, No. 5, p. 2441.
5. IEEE P1547 Std Draft 06 Standard for Distributed Resources Interconnected with Electric Power Systems, IEEE SCC21, 2000.
6. Francis, B. A. & Wonham, W. M. (1975). The internal mode principle for linear multivariable regulators, *Appl. Math. Opt*. Vol. 2, p. 170.
7. Teodorescu, R., Blaabjerg, F., Liserre, M. & Loh, P.C. (2006). Proportional-resonant controllers and filters for grid-connected voltage-source converters. *IEE Proc.-Electr. Power Appl*., Vol. 153, No. 5, p. 750.
8. Hasanzadeh, A. & Mokhtari, H. (2009). A simplified droop method implementation in parallel UPS inverters with proportional-resonant controller. *Iranian Journal of Science & Technology, Transaction B: Engineering*, Vol. 33, No. B2, pp. 163-178.
9. Slotine, J. J. & Li, W. (1990). *Applied nonlinear control*. Prentice-Hall
10. Ryan, M. J., De Doncker, R. W. & Lorenz, R. D. (2001). Decoupled control of a four-leg inverter via a new 4×4 transformation matrix. *IEEE Trans. Power Electron*., Vol. 16, No. 5, p. 694.
11. Baran, M. E. & El-Markaby, I. (2005). Fault analysis on distribution feeders with distributed generators, *IEEE Trans. Power Sys*. Vol. 20, No. 4, p. 1757.
12. Astrom, K. J., Wittenmark, B. (1990). *Computer-controlled system*. second ed., Prentice-Hall, Inc.
13. Mohan, N., Undeland, T. M. & Robbins, W. P. (2003). *Power electronics*. third ed., John Wiley & Sons, Inc.

14. Prodanovic, M. & Green, T. C. (2003). Control and filter design of three-phase inverters for high power quality grid connection. *IEEE Trans. Power Elec*., Vol. 18, No. 1, p. 373.
15. Wang, C., Nehrir, M. H. & Gao, H. (2006). Control of fuel cell distributed generation systems. *IEEE Trans. Energy Conv*., Vol. 21, No. 2, p. 586.