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BANDWIDTH OPTIMIZATION TO ACHIEVE MINIMUM PHASE NOISE IN FREQUENCY SYNTHESIZERS*

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Abstract– This paper analyzes the phase noise of the single loop second-order frequency fractional-N synthesizer. The aim of this paper is the reduction of the output phase noise in the application of commercial and military subsystems as well as general local oscillators. The mathematical model of PLL based frequency synthesizer is analyzed to develop the minimum phase noise in the specific frequency range. An exact closed form relationship between bandwidth and output phase noise of the frequency synthesizer as well as the bandwidth-phase noise diagram is extracted by using this closed form relationship. From the analysis and simulation results, we observe that the system has minimum phase noise at a particular closed-loop bandwidth. To validate simulation results, the synthesizer is implemented on the low loss professional printed circuit board (PCB). Measurement setup is scheduled on spectrum analyzer 8562A in the span of 5MHz and 10MHz. These measurements show excellent results in output spectrum of the frequency synthesizer.

Keywords– Frequency synthesizers, phase noise, phase-locked loop, phase noise reduction

1. INTRODUCTION

Frequency **sy**nthesizer is an important subsystem of any communication systems and radars. A frequency synthesizer is a device that generates one or many frequencies from one or a few frequency sources. Practically, all communication systems use local oscillator (LO) based on frequency synthesis. It is widely used in telecommunication receivers, transmitters and radar systems, as a part of the frequency conversion block. The receiver must be sensitive, selective, and able to detect even a weak signal among many other, possibly stronger signals [1]. Therefore, a good receiver must have an accurate frequency in the local oscillator and low-noise components. However, a transmitter must produce a signal that has enough power, very accurate frequency and clean enough spectrum.

One of the major issues facing synthesizer designers is the phase noise phenomenon. Phase noise is an undesirable entity that exists in all real world oscillators and signal generators. The term phase noise is used to describe phase fluctuations due to the random frequency fluctuations of signal. It can cause distortion or damage of incoming information in traditional receivers, and it introduces high bit error rates in modern broadcasting systems because phase deviations directly increase the occurrence of errors in bit detection. Therefore, it is necessary to understand and quantify phase noise so that those effects on the higher level product are minimized. Phase noise and those effects on the performance of synthesizer have been the subject of numerous studies [2-4].

Fortunately, phase noise is a manageable problem. Oscillator designers can work to minimize phase noise in oscillators, and synthesizer designers can better design their systems by choosing a low noise

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oscillator and other components of synthesizer. External noise and interference degrade the phase noise performance of synthesizers, and engineers need to be aware of these factors so that their effects can be anticipated or avoided. It is important to obtain the advanced phase noise model for frequency synthesizer used in the broadcasting service transmitting system and receiving terminals, in prediction of phase noise effects and/or design of signal sources with low phase noise. The typical way of predicting the noise performance of the synthesizer is based on the linear phase-domain models that are described in locked state [3, 5].

In section 2, we describe the structure of Σ-Δ charge pump PLL (phase locked loops) and its behavioral model. The third section represents the noise contribution in PLL and PSD of each noise source. In section 4, a mathematical method has been given to find a closed-form relationship for phase noise of the synthesizer. In section 5, we simulate the mathematical results obtained in previous sections and draw the curve of total output phase noise as a function of bandwidth and discuss some details about it. Finally, in section 6 we present the measurement results of a constructed circuit of a S-band synthesizer.

2. BACKGROUND

a) Structure of charge-pump PLL

Figure 1 displays a block diagram of a typical Σ-Δ frequency synthesizer. It consists of four basic building blocks: phase/frequency detector (PFD), loop filter, voltage controlled oscillator (VCO) and frequency divider. The synthesizer works in a phase-locked loop (PLL), where the PFD compares the phase of the reference signal (Φ_{ref}) and divided feedback signal (Φ_{div}).

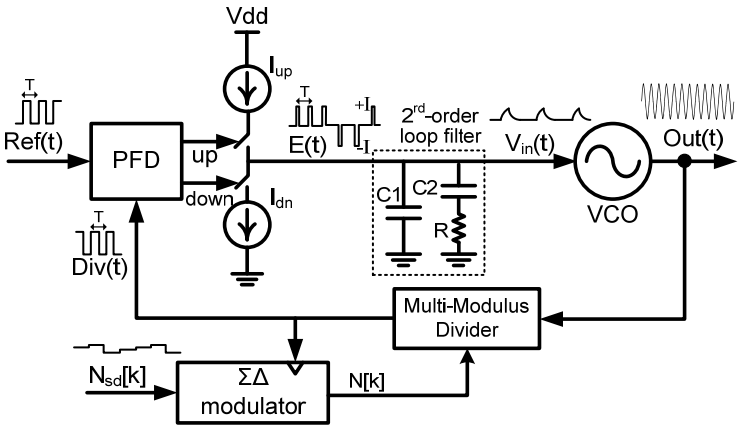

Fig. 1. Block diagram of fractional-n frequency synthesizer [11]

The PFD's outputs are proportional to the input signals phase and frequency difference. These output signals (up and down) are fed to the charge pump, where they control the charge pump sink (I_{dn}) and source (I_{up}) currents. If $f_{ref} > f_{div}$, the up signal will be non-zero and turn on its associated switch intermittently, while the down pulse will be zero continuously. This will inject positive charges into the loop filter, which in turn results in an increase in the output voltage, V_{tune}, to adjust the VCO frequency. If $f_{ref} < f_{div}$, it is vice versa of the above process.

The charge pump output current is converted to VCO control voltage through the loop filter to drive an external voltage-controlled oscillator (VCO) to increase or decrease the output frequency so as to drive the PFD's average output towards zero. The loop filter attenuates high-frequency components in the PFD output so that a smoothed error signal is sent to the VCO input. It is to be noted that in charge pump PLLs, the minimum order of the loop filter must be two [3]; therefore, the simplest and most usual architecture

of loop filter was used in our system. The output frequency is fed back to the PFD through the divider. The loop reaches locked states when the reference and divided output signals have the same frequency and phase. Since charge pump is a discrete-time system, as long as the dynamics of the loop are much slower than the signal, it can be considered as a continuous-time system [6]. Therefore, in designs, the loop bandwidth has to determine between 0.02 and 0.1 of input frequency. Thus, by using average value of discrete-time parameters, the PLL can be analyzed as a continuous-time system [7]. Exact analysis of charge pump PLL is given in [8].

As shown in Fig. 1, a sigma delta modulator (SDM) is used to change the value of the frequency division at a high rate compared to the bandwidth of PLL so that, over time, the frequency is effectively divided by an average value that is fractional rather than integer. The resolution of these fractional values is determined by the length of the accumulators making up the SDM. To overcome the spurious signal generation problem, a fractional frequency synthesizer can exploit noise shaping in a Multi-stAge noise SHaping (MASH) SDM in a similar way so that analog to digital conversion utilizes this behavior. In a typical frequency synthesizer the low-pass filtering operation is carried out on the quantization noise by the loop filter [9-10]. A third order MASH Σ−Δ modulator is used in this design that exhibits by a 3rd-order noise transfer function and a 5-bit output.

b) Behavioural model

In order to reveal the noise contribution in the PLL based synthesizer, it is necessary to have a model in which the effect of each noise source into output phase noise can be analysed. The transient response of the PLL is generally nonlinear, and cannot be formulated. But, in locked condition, the PLL acts as a LTI system and hence the superposition holds. The linear model, depicted in Fig. 2, is used to analyze the behavior of the ΣΔ synthesizer in locked condition [11]. It is very useful for PLL stability and phase noise contribution analysis [12]. Note that this linearized model can be used to analyze the "small signal" dynamic properties of the PLL as well as its noise performance; that is, only variations in the PLL frequency caused by small changes in the divider value are considered. If the divider value is large, then cycle slip may occur and thereby invalidate our modeling assumptions [11].

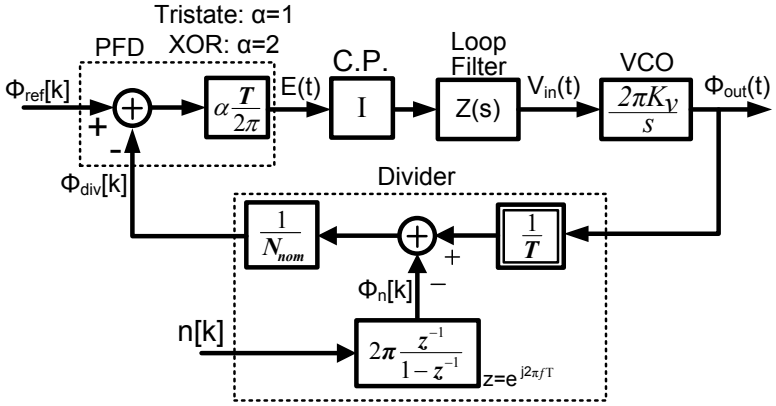

Fig. 2. Behavioral model of a typical frequency synthesizer

Fortunately, for most practical cases the frequency change is slow enough to avoid losing frequency lock. In the locked state the phase of the reference source Φ_{ref} and divided VCO signal Φ_{div} are the same. The phase is the parameter of interest and phase characteristics for every block has to be derived.

The loop-filter transfer function, Z(s), is defined as the ratio of its output voltage to its input current. Equations for different loop filter architectures and the theory of their design can be found in [13]. In

general, the loop filter design is one of the most critical parts of the synthesizer design. From the point of noise, passive filters only introduce white noise due to resistors whereas active filters usually contain additive 1/f noise. This noise component is due to active devices (such as op-amp) in these filters.

In this study, we consider a PLL with type II and order of 2 that are fairly standard values for practical broadcasting systems. Therefore, as shown in Fig. 1 the transfer function of desired loop filter (lead/lag) will be in the following form:

$$Z(s) = \frac{1}{sA_0} \cdot \frac{1 + sT_2}{1 + sT_1} \tag{1}$$

where $A_0=C_1+C_2$, $T_1=RC_1C_2/(C_1+C_2)$, and $T_2=1/RC_1$. This filter is convenient for most synthesizer applications due to the prohibitively high analog complexity required to achieve higher order or higher type values.

3. PHASE NOISE MODEL AND ANALYSIS

a) Noise sources

The noise sources in all building blocks of the PLL contribute to the noise power spectral density of output signal. Noise sources in the circuit can be divided into two groups, namely device noise and interference. Thermal, shot and flicker noises are examples of the former, while substrate and supply noise are in the latter group [14].

Each component of PLL introduces different types of noises. These noises are due to active or passive devices employed in the blocks. In order to characterize the output phase noise of the synthesizer, it is necessary that first the noise properties of individual block of the synthesizer be identified, and then those influences are evaluated on the output phase noise.

Figure 3 displays the noise contribution of individual block of the synthesizer as additive noise. In this paper we assume that four noise sources appear in the PLL which are originated by PFD, charge pump, voltage-controlled oscillator, and Σ-Δ quantization noise. These noises pass through individual transfer function and affect the output frequency spectrum of the synthesizer. Since these noise sources are small (compared with the desired signal) and uncorrelated to each other, and behavioral model is linear as well, the output phase noise power spectrum density (PSD) is calculated by multiplying the input power spectrum density of noise sources, $S_{\varphi\text{-source}}(f)$, by the associated magnitude square of closed-loop transfer function, $F_{source}(f)$, which is defined as ($F_{source} = \phi_{out}/S_{\varphi\text{-source}}$).

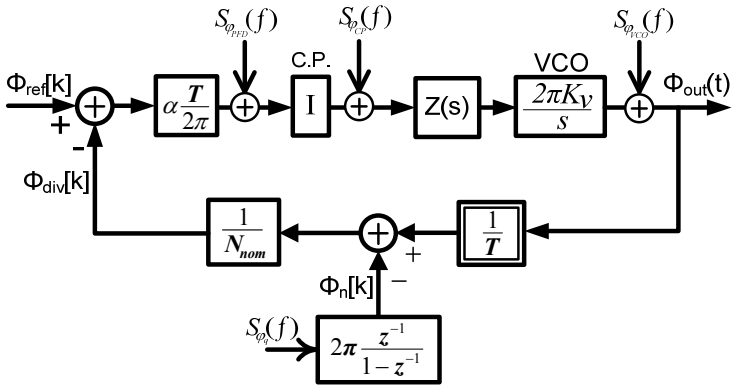

Fig. 3. Noise contribution in the fractional synthesizer

The position of the input noise sources vary depending on the investigating noise. It determines the ability of the system to terminate phase noise. The total output phase noise PSD of the synthesizer is given as follows:

$$S_{out}(f) = \sum_{all\ sources} S_{source}(f) \cdot \left|F_{source}(f)\right|^2 \tag{2}$$

By using superposition law, the total output phase noise will be the sum of the Eq. 2 on all noise sources as follows:

$$\begin{aligned} S_{\varphi\text{-}output}(f) = {} & S_{\varphi,PFD}(f) \cdot |F_{PFD}(f)|^2 + S_{\varphi,CP}(f) \cdot |F_{CP}(f)|^2 \\ & + S_{\varphi,VCO}(f) \cdot |F_{VCO}(f)|^2 + \frac{1}{T} S_{\varphi\text{-}q}(f) \cdot |F_q(f)|^2 \end{aligned} \tag{3}$$

The term 1/T at the end of Eq. (3), is the discrete-time signal, $S_{\varphi\text{-}q}(f)$, which is applied to a continuous-time system [10]. To continue, the properties of each noise source is investigated.

1. VCO noise: Many studies have been performed to characterize the VCO phase noise [15, 16]. In frequency domain the PSD of VCO noise model can be written as follows:

$$S_{\varphi,VCO} = k_{0,VCO} + \frac{k_{2,VCO}}{f^2} + \frac{k_{3,VCO}}{f^3} \tag{4}$$

According to the above equation, the noise prototype of the actual VCO has three sections that correspond to 0 dB/dec, -20dB/dec, and -30dB/dec slopes. The VCO deviates from the -20dB/dec roll-off at low frequencies due to flicker noise, and at high frequencies due to white noise floor. However, the assumption of -20dB/dec roll-off suffices for the frequency offsets of interests.

2. PFD/CP Noise: The PFD's have an intrinsic noise in the white and flicker form. If special attention is not paid to their design, PFDs will be still susceptible to noise, particularly, $1/f$ noise, substrate and supply noise. Their noise properties have been studied to some extent in [3]. In the behavioral simulations, we assume that the charge-pump noise magnitudes are approximately equal for positive and negative current sources. So, it is approximated by variance of up and down current sources which are in the white noise form.

3. Σ-Δ Quantization Noise: The spectrum of the quantization noise is shaped according to the order and architecture of the Σ−Δ topology employed. We assume that a MASH structure [17] is sampled at a rate equal to the reference frequency. Thus, the quantization noise changes continuously and it can be represented statistically as a white noise source [18]. In general, modeling of a Σ-Δ modulator is accomplished by assuming its quantization noise is independent of its input. This leads to a linear time-invariant model that is parameterized by transfer functions from the input and quantization noise to the output. For instance, a MASH Σ-Δ modulator structure of order *m*, input *x[k]*, and output *y[k]* is described by:

$$y(z) = x(z) - (1 - z^{-1})^m r(z) \tag{5}$$

where $r[k]$ is quantization noise, that is shaped by the filter $(1\text{-}z^{-1})^m$ and appears in front of the main divider. Quantization noise transfer function is a main performance factor of SDMs. In the 3rd-order MASH type, the quantization error noise spectrum is shaped by the transfer function given in the following [11]:

$$S_{\varphi-q}(f)=\frac{1}{12}(1-z^{-1})^3 \tag{6}$$

By substituting $Z^{-1}=e^{-j2\pi fT}$ in the above equation we have:

$$S_{\varphi-q}(f)=\frac{1}{12}(2\sin(\pi fT))^6 \tag{7}$$

b) Analysis

Now, the transfer function of individual noise source should be specified. To parameterize these transfer functions, it is convenient to define a base function that provides a simple description of all the PLL transfer functions of interest. If we define A(f) as the open loop transfer function of the PLL, the following function, G(f), works well for this purpose.

$$G(f)=\frac{A(f)}{1+A(f)} \tag{8}$$

where A(s) is the open loop transfer function in Fig. 3 as follows:

$$A(s)=\left(\frac{\alpha}{2\pi}\right)\cdot I\cdot Z(s)\left(\frac{2\pi K_v}{s}\right)\left(\frac{1}{N_{nom}}\right)\Bigg|_{s=j2\pi f} \tag{9}$$

The magnitude square of closed-loop transfer function of each noise source (mentioned in Eqs. (2) and (3) as $F_{source}(f)$) is derived from Fig. 3 as:

$$\left|F_{PFD}(s)\right|^2=\left|\frac{\phi_{out}(s)}{S_{PFD}(s)}\right|^2=\left|\frac{2\pi}{\alpha}\cdot N_{nom}\cdot G(s)\right|^2 \tag{10}$$

$$\left|F_{CP}(s)\right|^2=\left|\frac{\phi_{out}(s)}{S_{CP}(s)}\right|^2=\left|\frac{1}{I}\cdot\frac{2\pi}{\alpha}\cdot N_{nom}\cdot G(s)\right|^2 \tag{11}$$

$$\left|F_{VCO}(s)\right|^2=\left|\frac{\phi_{out}(s)}{S_{VCO}(s)}\right|^2=\left|1-G(s)\right|^2 \tag{12}$$

$$\left|F_{q}(s)\right|^2=\frac{1}{T}\left|\frac{\phi_{out}(s)}{S_{q}(s)}\right|^2=\frac{1}{T}\left|2\pi\frac{z^{-1}}{1-z^{-1}}\cdot T\cdot G(s)\right|^2 \tag{13}$$

So, the output phase noise curve of the synthesizer can be derived by use of Eq. (3). Figure 4 depicts the output phase noise due to each noise source as well as the total output phase noise. It is clear from Fig. 4 that the output phase noise is mainly influenced by the VCO phase noise for high offset frequency range and phase noise of the PFD for low offset frequency range. Therefore, to simplify later calculations, we can rewrite the total output phase noise in terms of VCO noise and PFD noise only. So, by use of (3), (8), and (10)-(18) the total output phase noise will be written as follows:

$$S_{out}(f)=S_{pfd}\cdot\left|2\pi NG(f)\right|^2+S_{vco}(f)\cdot\left|1-G(f)\right|^2 \tag{14}$$

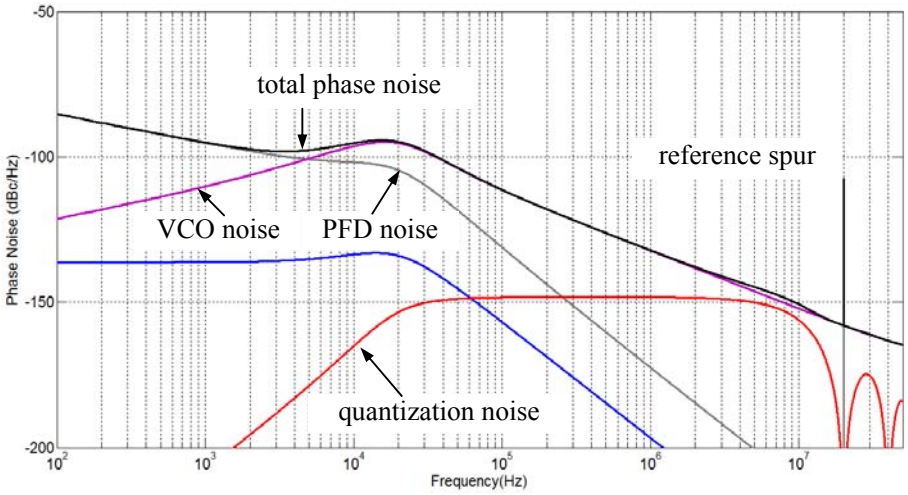

Fig. 4. Phase noise characteristic of frequency synthesizer

4. PARAMETERIZATION OF SYNTHESIZER

In this section, we attempt to find a closed form relation between total output phase noise ($S_{out}(f)$) and the closed-loop bandwidth of the synthesizer, i.e. ω_c. For this reason, G(f) in (12) must be extracted only as a function of the bandwidth of the system. According to Eq. (8), G(f) is in terms of A(f) only, and therefore, A(f) must be extracted in terms of the bandwidth only.

Substituting (1) into (9) and arranging, we have:

$$A(s)=\frac{I\cdot K_v}{N\cdot s}\cdot\frac{1}{s\cdot A_0}\cdot\frac{1+sT_2}{1+sT_1} \tag{15}$$

If φ be phase margin of the loop, we have:

$$\tan^{-1}(\omega_c T_2)-\tan^{-1}(\omega_c T_1)=\varphi \tag{16}$$

Tangent of the angle φ in the above equation could be written as:

$$\frac{\omega_c\left(T_2-T_1\right)}{1+\omega_c^2 T_1 T_2}=\tan\varphi \tag{17}$$

In the PLL design, it is highly desirable to let the maximum phase of the open loop transfer function, $\angle A(j\omega)$, occur at the magnitude crossover frequency ω_c in order to obtain the maximum phase margin. In addition, at the maximum point the first order derivative of the phase is zero, which implies the phase margin has a least sensitivity to the loop parameter variation. The phase of A(s) is:

$$\theta=\angle A(j\omega)=-180+\tan^{-1}(\omega T_2)-\tan^{-1}(\omega T_1) \tag{18}$$

Let $\left.\frac{d\theta}{d\omega}\right|_{\omega=\omega_c}=0$, to obtain the following equation:

$$\omega_c=\frac{1}{\sqrt{T_1 T_2}} \tag{19}$$

By combining (17) and (19) we have:

$$\sqrt{\frac{T_2}{T_1}} - \sqrt{\frac{T_1}{T_2}} = 2\tan\varphi \tag{20}$$

Equation (20) can be written as:

$$\eta + \frac{1}{\eta} = 2 + 4\tan^2\varphi \tag{21}$$

where $\eta = \frac{T_2}{T_1}$. Furthermore, using (19) we can write:

$$T_1 = \frac{1}{\omega_c\sqrt{\eta}} \quad , \quad T_2 = \frac{\sqrt{\eta}}{\omega_c} \tag{22}$$

Since in the bandwidth frequency, the magnitude of the open loop transfer function is equal to one, i.e. $|A(j\omega_c)|=1$, the constant A_0 is obtained as follows:

$$A_0 = \frac{IK_v}{N\omega_c^2}\cdot\frac{\sqrt{1+(\omega_c T_2)^2}}{\sqrt{1+(\omega_c T_1)^2}} = \frac{IK_v\sqrt{\eta}}{N\omega_c^2} \tag{23}$$

Solving the second order equation in (21), two possible values for η are achieved. Since η is the pole to zero ratio of the loop filter which is always more than 1 for stable systems, we can select one of two answers of Eq. (21) as follow:

$$\eta = \frac{2 + 4\tan^2\varphi + \sqrt{(2+4\tan^2\varphi)^2 - 4}}{2} \tag{24}$$

Now, by substituting (22), (23) into (16), the open loop transfer function, A(f), will be expressed in terms of the closed-loop bandwidth and η only:

$$A(f) = \frac{IK_v}{jN2\pi f}\cdot\frac{N\omega_c^2}{j2\pi f IK_v\sqrt{\eta}}\cdot\frac{1+s\sqrt{\eta}/\omega_c}{1+s/\omega_c\sqrt{\eta}} \tag{25}$$

where η is obtained from Eq. (24).

5. SIMULATION RESULTS AND DISCUSSION

Figure 5 shows the curve of the total output phase noise for several closed loop bandwidths in phase margin of 45°. Each curve has a local maximum around its designed bandwidth frequency. In 4KHz bandwidth, the phase noise PSD at low offset frequencies is large. If the closed loop bandwidth is increased, the local maximum point is shifted into higher offset frequencies. However, this figure cannot show which bandwidth gives the minimum phase noise, since by increasing the bandwidth of the system, the phase noise increases in some regions and decreases in another region (e.g. 20KHz and 200KHz bandwidth in Fig. 5).

To evaluate the effect of various bandwidths on the total output phase noise, we calculate the phase noise power in a particular frequency range for individual bandwidth. In fact, we evaluate the phase noise power instead of the phase noise power density. To find the phase noise power, the PSD of phase noise is integrated with interested frequency range (f_1~f_2). It may be written as Eq. (23). In this paper, interested frequency region is from 1Hz to 1MHz.

$$P_{noise_{out}} = \int_{1}^{10^6} S_{out}(f)df \tag{26}$$

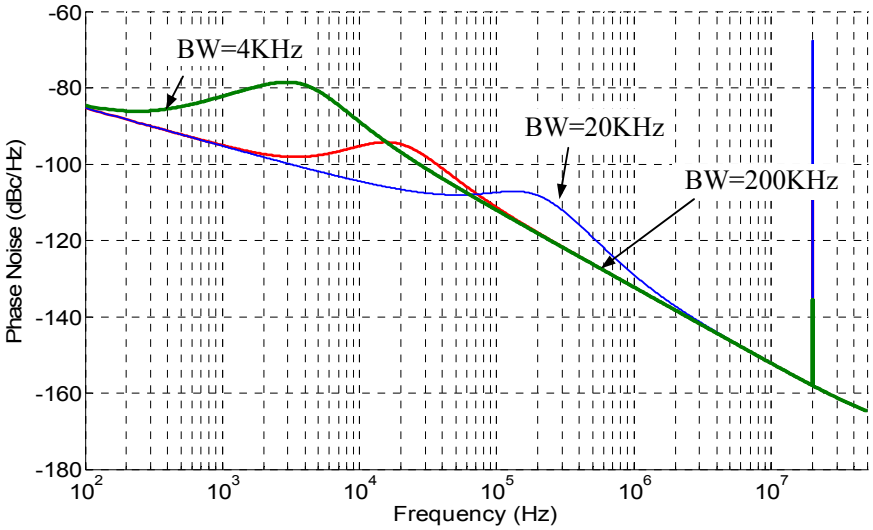

Fig. 5. Total output phase noise in bandwidth of 4KHz, 20KHz, and 200KHz

Figure 6 shows the phase noise power as a function of closed loop bandwidth. As seen, there is an optimum closed loop bandwidth for minimization of phase noise of the synthesizer. In 100KHz bandwidth, we achieve minimum phase noise power. Practically, selecting the bandwidth in the limit of 30KHz up to 200KHz is appropriate for many applications. In this limit, larger bandwidth leads to faster lock time but larger reference spur. Furthermore, the loop bandwidth must be between 0.02 and 0.1 of input frequency to accomplish stability considerations.

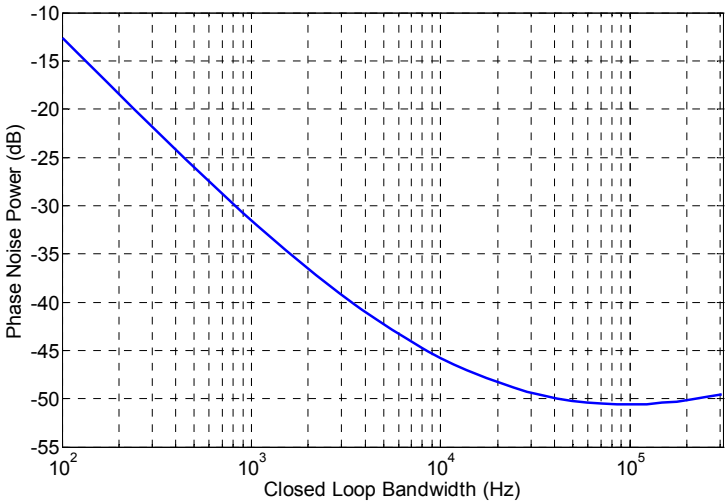

Fig. 6. Total phase noise power for closed loop bandwidth

6. MEASUREMENT RESULTS

As shown in Fig. 7, the designed system with 20KHz bandwidth is mounted on the RF prototype board. Taking into account the range and stepping of the output frequency, an integrated chip ADF4154 is selected as the phase frequency detector. ADF4154 is a highly integrated charge-pump type fractional-N frequency synthesizer chip. The normalized phase noise floor of -220 dBc/Hz (at 100KHz offset) and maximum operating frequency of 4GHz are two of its specifications [19]. There are phase frequency

detector (PFD), charge pump, reference frequency divider, programmable A and B counters and dual-modulus prescaler included in the integrated chip. A crystal oscillator of 20MHz made in Rakon company is chosen as a reference signal source. A voltage-controlled oscillator of JTOS3000P is used. This VCO covers the frequency range of 2.3GHz up to 2.6GHz.

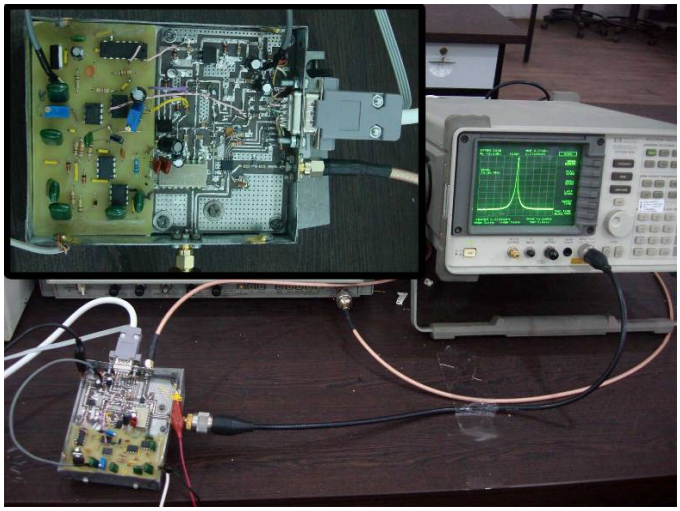

Fig. 7. Fractional-N synthesizer mounted on a professional board

We tested the actual circuit performance and the phase noise results are matched with simulations. Figure 8 shows measured plot of the output spectrum in the frequency of 2.4454GHz. The plot was obtained from an HP-8562A spectrum analyzer for 5 and 10MHz span frequencies. A common way of measuring phase noise using a spectrum analyzer is as follows:

$$(PN)_{dB} = -(CP)_{dB} + (NP)_{dB} - 10 \cdot \log(RB) \tag{27}$$

where PN, CP, NP and RB are phase noise, carrier power, noise power and resolution bandwidth respectively. As observed in Fig. 8, the resolution bandwidth (RBW) of spectrum analyzer has been adjusted at 30 KHz and the carrier power is equal to 9dBm**.** To obtain the phase noise of this signal at 500KHz offset for example, we read the noise power at 500KHz about -70dBm (in the left panel of Fig. 8). Therefore, the phase noise is: $-9^{dBm}-70^{dBm}-10\log(30\times10^3)\approx-123.7$dBc/Hz, that is the same as the phase noise of the corresponding curve (i.e.: BW=20KHz) in Fig. 5 at 500KHz. The resulting spectra compare quite well with the total phase noise calculated in Fig. 5 for bandwidth of 20KHz over the frequency offset range of 25 kHz to 5MHz.

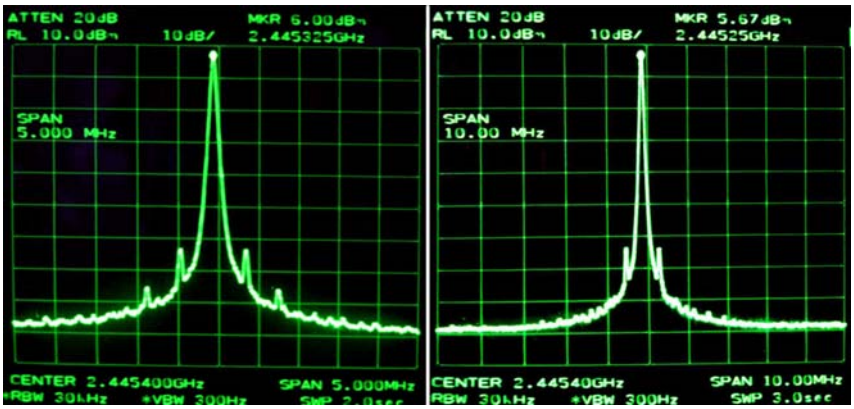

Fig. 8. Output spectrum of the frequency synthesizer in the span of 5MHz (left) and 10MHz (right)

7. CONCLUSION

This paper addressed the phase noise of the ΣΔ frequency synthesizer with second-order passive loop filter. A mathematical and accurate model for phase noise of the frequency synthesizer was presented taking into account noise of its components. Noise sources are: phase /frequency detector, charge pump, VCO, and Σ-Δ quantization noise. Then, output phase noise was predicted in terms of these parameters. A closed-form relationship between the output phase noise and closed loop bandwidth of the synthesizer was also extracted. Finally, the value of optimal closed loop bandwidth minimizing the phase noise was obtained in phase noise analysis. In addition, a prototype synthesizer has been implemented on a professional board and output phase noise was analyzed in several bandwidths. Results were excellent.

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